REMARKS

Claims 1-8 are pending in this application. Claims 1 and 5 are independent. In light of the remarks contained herein, Applicants respectfully request reconsideration and withdrawal of the outstanding rejections.

In the outstanding Official Action, the Examiner rejected claims 1 and 2 under 35 U.S.C. § 102(a) and (b) as being anticipated by Yamasaki, et al. (USP 5,539,916); and rejected claim 5 under 35 U.S.C. § 102(a) and (b) as being anticipated by Tsuboi, et al. (USP 5,140,582). Applicants respectfully traverse these rejections.

Applicants wish to thank the Examiner for indication that claims 3-4 and 6-8 contain allowable subject matter.

Claims Rejections-35 U.S.C. § 102(a) and (b) - Yamasaki, et al.

In the outstanding Official Action, the Examiner asserts that neither Applicants specification nor the claims distinguish self-synchronization from non-self-synchronization. Applicants respectfully disagree with this assertion. The Examiner's attention is respectfully directed to exemplary disclosure that provides a definition of a self-synchronous system on page 3, lines 1-10 and page 13, lines 24-33.

It is respectfully submitted that the invention set forth in claim 1 recites, *inter alia*, a self-synchronous transfer

control circuit comprising a pulse control circuit receiving one data transfer request pulse signal as the first pulse from the transfer control circuit in the proceeding stage to output a plurality of data transfer request pulse signals as the second pulse to the transfer control circuit in a subsequent stage.

It is respectfully submitted that the disclosure of Yamasaki, et al. is directed to a DMA control circuit for continuing transfer to input/output device in a cycle steal mode. Yamasaki, et al. provides transfer pulse generator 11 and request signal generator 10 where request signal generators outputs a bus request signal (BRQ), however Yamasaki, et al. fails to teach or suggest outputting a plurality of transfer request pulse signals as recited in claim 1. As Yamasaki, et al. fails to teach or suggest outputting a plurality of data transfer request pulse signals as the second pulse to the transfer control circuit in the subsequent stage, as recited in claim 1, it is respectfully submitted that Yamasaki, et al. fails to anticipate the present invention.

It is respectfully submitted that claim 2 is allowable for the reasons set forth above with regard to claim 1 at least based upon its dependency on claim 1.

Claim Rejections-35 U.S.C. § 102(a) and (b) - Tsuboi, et al

By this amendment, Applicants have amended claim 5, lines 6-7 to recite holding a data packet based on a pulse signal. This amendment is being made to more appropriately recite the present invention.

In support of the Examiner's rejection of claim 5, the Examiner asserts that Tsuboi, et al. teaches data transmission path for holding a data packet based on a clock signal. The Examiner states that this feature is not explicitly shown but that Tsuboi, et al.'s system must have this feature otherwise it would not work.

It is respectfully submitted that the present invention as set forth in claim 5, as amended, recites *inter alia*, a data driven information processing device comprising a data transmission path holding a data packet based on a pulse signal applied from the self-synchronous transfer control circuit. As admitted by the Examiner, Tsuboi et al. teaches holding a data packet based on a clock signal and not a pulse signal as recited in claim 5. As Tsuboi et al. fails to teach or suggest holding a data packet based on a pulse signal, it is respectfully submitted that Tsuboi et al. fails to teach or suggest the invention as recited in claim 5. Is is respectfully requested that the outstanding rejection be withdrawn.

Conclusion

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Catherine M. Voisinet (Reg. No. 52,327) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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